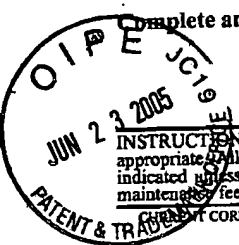


## PART B - FEE(S) TRANSMITTAL



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23494 7590 05/31/2005

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**Robina E. Barnum** (Depositor's name)  
*Robina E. Barnum* (Signature)  
**June 23, 2005** (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,731	11/15/2000	Timothy D. Anderson	TI-29298	3516

**TITLE OF INVENTION: INSTRUCTION-PROGRAMMABLE PROCESSOR WITH INSTRUCTION LOOP CACHE**

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$0	\$1400	08/31/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
PAN, DANIEL H	2183	712-033000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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- 1 Robert D. Marshall, Jr.  
 2 W. James Brady, III  
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**Texas Instruments Incorporated**

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Authorized Signature

*Robert D. Marshall, Jr.*

Date **June 23, 2005**

Typed or printed name

**Robert D. Marshall, Jr.**

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Timothy D. Anderson

Serial No.: 09/713,731

Filed: November 15, 2000

For: Instruction Loop Buffer

TI-29298

Art Unit: 2183

Examiner: Daniel H. Pan

Conf. No.: 3516

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 Robin E. Barnum

June 23, 2005  
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TITLE OF INVENTION: Instruction Loop Buffer		Serial No.: <b>09/713,731</b>	
TI FILE NO.: <b>TI-29298</b>		Filing Date: November 15, 2000	
DEPOSIT ACCT. NO.: <b>20-0668</b>			
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